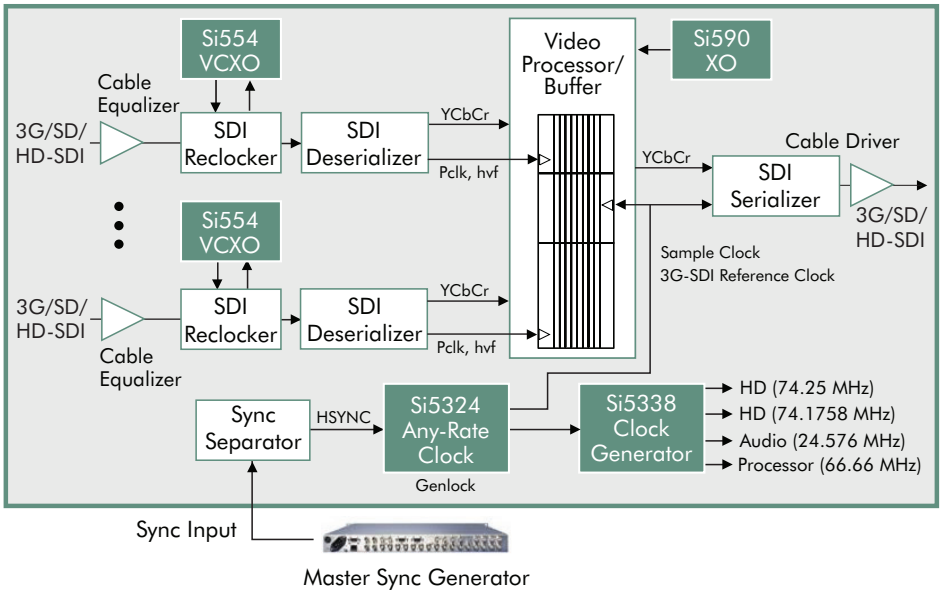
Video Timing Solutions

FULLY INTEGRATED, FREQUENCY FLEXIBLE GENLOCK SOLUTION

DESCRIPTION

Silicon Laboratories' Si5324 Any-Rate Precision Clock is the industry's lowest jitter, most highly integrated video clock IC optimized for genlock applications. Based on Silicon Labs' patented DSPLL® technology, the Si5324 has a fully integrated, digitally programmable loop filter that supports loop bandwidths ranging from 4 Hz to 525 Hz as well as a low phase noise internal VCO. By consuming less than 10% of the overall 3G-SDI jitter budget required in next generation video applications, the Si5324 simplifies design and eases system-level SDI jitter testing. In addition, the Si5324 provides any-rate frequency flexibility by generating virtually any output frequency from 2 kHz to 1.4 GHz from any input frequency ranging from 2 kHz to 710 MHz enabling a single IC design for multi-rate video applications.

Application Example: Production Video Switcher



FEATURES

- Generates any frequency from 2 kHz to 945 MHz and select frequencies to 1.4 GHz from an input frequency of 2 kHz to 710 MHz
- Ultra-low jitter 0.58 ps RMS, 5 ps pk-pk at 3G-SDI (10 Hz to 20 MHz)
- Digitally programmable loop bandwidth with fastlock (4 Hz to 525 Hz)
- Meets 3G-SDI (SMPTE 424M) for timing and alignment jitter limits
- Genlock, free-run, and digital hold
- Hitless switching between input clocks with phase build-out
- Manual or automatic (revertive, non-revertive) input clock selection
- LOL, LOS and FOS alarm outputs
- Configurable signal format per output (LVPECL, LVDS, CML, CMOS)
- I²C/SPI programmable
- Single supply 1.8, 2.5 or 3.3 V ±10% with high PSNR
- Pb-free, RoHS compliant

APPLICATIONS

- Video or audio genlock and synchronization
- FPGA SDI SerDes recovered clock generation
- Triple rate 3G/HD/SD-SDI SerDes
- Video capture, conversion, editing and distribution
- Digital audio or video recording and playback devices
- Video server
- Video format converter
- Video switcher and frame synchronizer

SOLUTIONS GUIDE

ANY-RATE
FREQUENCY SYNTHESIS
IN A SINGLE IC

SILICON LABS

ANY-RATE FREQUENCY FLEXIBILITY

High Performance

The Si5324 is the industry's lowest jitter genlock clock IC. The device provides any-rate frequency synthesis simplifying HD video and audio clock generation. With jitter performance of 5 ps pk-pk, the Si5324 delivers significant jitter margin in 3G-SDI serializer applications, reducing design risk and improved link performance.

Highly Integrated

The Si5324 offers the industry's most highly integrated video clock generator IC requiring no external PLL components (low pass filter, charge pump, or VCXO). Because all PLL components are integrated, board-level noise immunity is improved reducing design risk versus traditional video clock IC solutions.

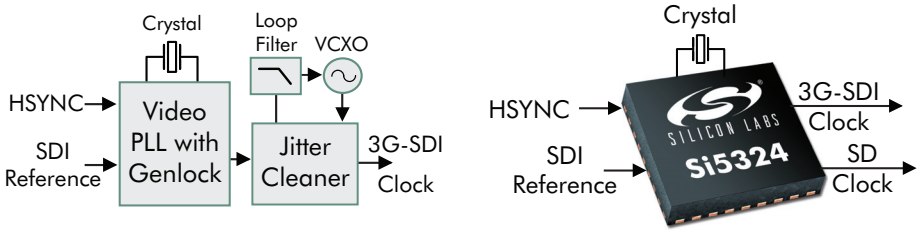
Any-Rate Frequency Flexibility

The Si5324's any rate frequency flexibility enables a single device to generate all common genlock reference frequencies required in next-generation SD/HD video and audio equipment. The Si5324 is easily reconfigurable via I2C/SPI interface and requires no component changes for different frequency plans, simplifying design reuse.

Industry's Most Integrated Genlock Solution

Silicon Labs' Si5324 replaces multi-component video clock ICs, external loop filter and VCXO components with a single IC, simplifying genlock designs.

Traditional Video Clock Solution vs. Silicon Labs Solution



Industry's Only Quad and Any-Rate Frequency XO/VCXOs

Si534 XO/Si554 VCXO

- Eliminates multiple oscillators, reduces system cost
- Simplifies BOM and saves board space and inventory
- Ideal for multi-rate FPGA-based PLLs

Built to Order Samples

Silicon Labs offers an easy-to-use web utility to build and configure the right XO/VCXO for your application. Samples of any frequency XO/VCXO are available in less than two weeks. **www.silabs.com/BuyXO**

2 WEEK LEAD TIMES

Recommended Silicon Labs Timing Solutions for Video

Any-Rate Jitter Attenuating Clock Multipliers, Clock Generators and Buffers

Part Number	Input/ Output Clocks	Control	Input Frequency	Output Frequency	Jitter	Minimum PLL Bandwidth	Jitter Attenuation	Clock Generation	Clock Distribution	Package
Si5324	2/2 Diff	I²C or SPI	2 kHz to 710 MHz	2 kHz to 1.4 GHz	5 ps pk-pk	4 Hz	•	•	•	36-QFN
Si5368	4/5 Diff	I²C or SPI	2 kHz to 710 MHz	2 kHz to 1.4 GHz	8 ps pk-pk	60 Hz	•	•	•	100-TQFP
Si5338	4/4 Diff	I²C or SPI	8 to 30 MHz (xtal) 160 kHz to 710 MHz (clock)	160 kHz to 710 MHz	36 ps pk-pk	1.6 MHz		•	•	24-QFN
Si5330	1:4 Diff 1:8 SE	Pin	5 to 710 MHz Diff 5 to 350 MHz SE	5 to 710 MHz Diff 5 to 350 MHz SE	55 fs rms	—			•	24-QFN

Single and Multi-Frequency Crystal-Based XO/VCXO

Part Number	Type	Frequency	Control	Frequency Range	Jitter	Stability/APR Options (ppm)	Kv Options (ppm/V)	Package
Si530/1	XO	Single	Pin	10 to 945 MHz 970 to 1134 MHz 1213 to 1417 MHz	0.3 ps rms	±20 ±31.5 ±61.5	N/A	6-pad
Si532/3	XO	Dual	Pin				N/A	6-pad
Si534	XO	Quad	Pin				N/A	8-pad
Si550	VCXO	Single	Pin	10 to 945 MHz 970 to 1134 MHz 1213 to 1417 MHz	0.5 ps rms	±12 to ±375	33 to 356	6-pad
Si552	VCXO	Dual	Pin					6-pad
Si554	VCXO	Quad	Pin					8-pad
Si570	XO	Programmable Any-Rate	I²C	10 to 280 MHz 10 to 810 MHz 10 to 1417 MHz	0.3 ps rms	±31.5; ±61.5	N/A	8-pad
Si571	VCXO	Programmable Any-Rate	I²C		0.5 ps rms	±12 to ±375	33 to 356	8-pad
Si590/1	XO	Single	Pin	10 to 525 MHz	0.7 ps rms	±30; ±50; ±100	N/A	6-pad
Si595	VCXO	Single	Pin		0.7 ps rms	±10 to ±370	45 to 380	6-pad

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